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Research Article

Two-Dimensional Tin Perovskite Photoelectric Transistor for High-Performance Photoelectric Controlled MOS Inverter

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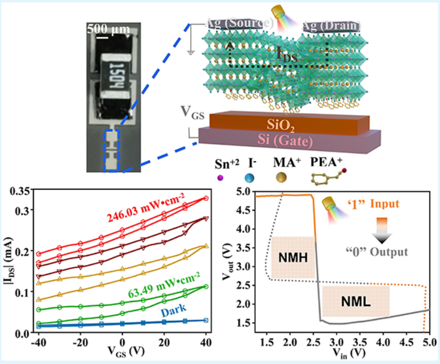

ABSTRACT: Two-dimensional (2D) tin (Sn) halide perovskites (HPs) are promising semiconductor materials for environmentally friendly lead-free photoelectric transistors. Herein, 2D perovskites $(PEA)_2MA_{n-1}Sn_nI_{3n+1}$ are successfully prepared by introducing large phenylethylamine (PEA) cations. The effect of the dimensional structure on the photoelectric performances of $(PEA)_2MA_{n-1}Sn_nI_{3n+1}$ is investigated. The electrical performances of $(PEA)_2MA_{n-1}Sn_nI_{3n+1}$ photoelectric transistors are significantly improved by regulating the dimensional microstructure of the perovskites. The $(PEA)_2MA_6Sn_7I_{22}$ ($n = 7$) photoelectric transistor shows n-type charge transport and excellent electrical properties with a linear mobility of 11.8 $cm^2 \cdot V^{-1} \cdot s^{-1}$, with a low subthreshold swing (SS) of 0.38 V·decade^{-1} and a detectivity (D^*) of 2.6×10^8 Jones. The standard deviation of performance parameters across 6 batches is less than 0.1 exhibiting a high level of consistency in device performance from batch to batch and good reproducibility. When stored in an N_2 glovebox for 15 days, the electron mobility of the device remained at 5.96 $cm^2 \cdot V^{-1} \cdot s^{-1}$, confirming their good long-term reliability. Additionally, the photoelectrically controlled metal−oxide−semiconductor (MOS) inverter is constructed by connecting the $(PEA)_2MA_6Sn_7I_{22}$ photoelectric transistor with a resistor, thus enabling logic values to be converted via photoelectric control at a low on-power consumption of 18 μW. The gain of the inverter was still maintained at 30 under varying test conditions, exhibiting remarkable stability. The developed high-gain photoelectric controlled MOS inverter with low energy consumption is applicable to portable electronic circuits.

KEYWORDS: *$(PEA)_2MA_{n-1}Sn_nI_{3n+1}$ perovskites, photoelectric transistors, photoelectric performances, photoelectric controlled MOS inverter*

1. INTRODUCTION

Photoelectric transistors have received significant attention owing to their wide applications.[1,2] Two-dimensional (2D) halide perovskites (HPs) exhibit outstanding carrier mobility, adjustable band gap, and light absorption properties, and have been extensively applied in photoelectric transistors.[3,4] In particular, 2D HPs are effective photoactive components that serve as conductive channels in photoelectric transistors and can achieve high flexibility and efficiency.[5,6] Lead-containing perovskite-based optoelectronics have developed rapidly; however, some critical problems remain to be resolved for their wide application, including lead toxicity and instability.[7] Tin (Sn) is highly similar to Pb, and the incorporation of Sn can reduce the toxicity of Pb.[8] Tin (Sn) is highly similar to Pb due to the similar outer electronic configuration (ns^2 np^2) and ionic radius (135 pm) of Sn to that of Pb (149 pm).[9] Besides, Sn-based perovskite exhibits an ideal band gap (1.3−1.4 eV) and high carrier mobility.[10] The incorporation of Sn can reduce the toxicity of Pb. Thus, Sn is a promising substitute for Pb.[11] Sn replacement has promoted the study of lead-free perovskite-based transistors.

2D phenethylammonium tin iodide perovskite ($(PEA)_2SnI_4$) was first used as the conductive channel of the field-effect transistor (FET) with a hole mobility of 0.6 $cm^2 \cdot V^{-1} \cdot s^{-1}$ in 1999.[12] Subsequently, researchers have attempted to improve the performance of transistors through thin-film crystallization, material, and structural engineering.[13,14] Senanayak et al. have reported that mixed metal (Pb/Sn) perovskite-based FET exhibits hysteresis-free p-type transport with a mobility of 5.4 $cm^2 \cdot V^{-1} \cdot s^{-1}$.[15] Liu et al. improved the mobility of a $(PEA)_2SnI_4$ FET from 0.25 to 0.68 $cm^2 \cdot V^{-1} \cdot s^{-1}$ by using solution doping technology.[16] Zhu et al. have reported a high-performance pure-Sn perovskite FET with a hole mobility exceeding 70 $cm^2 \cdot V^{-1} \cdot s^{-1}$ achieved via cation engineering.[17] Sn-based perovskite transistors exhibit better properties than Pb-based perovskite transistors, because Sn has a higher charge carrier mobility than Pb owing to its smaller atomic mass.[7] 2D Sn-based perovskites have large band gaps and exhibit quantum confinement effects.[18,19] By optimizing the material structure,

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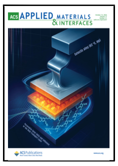

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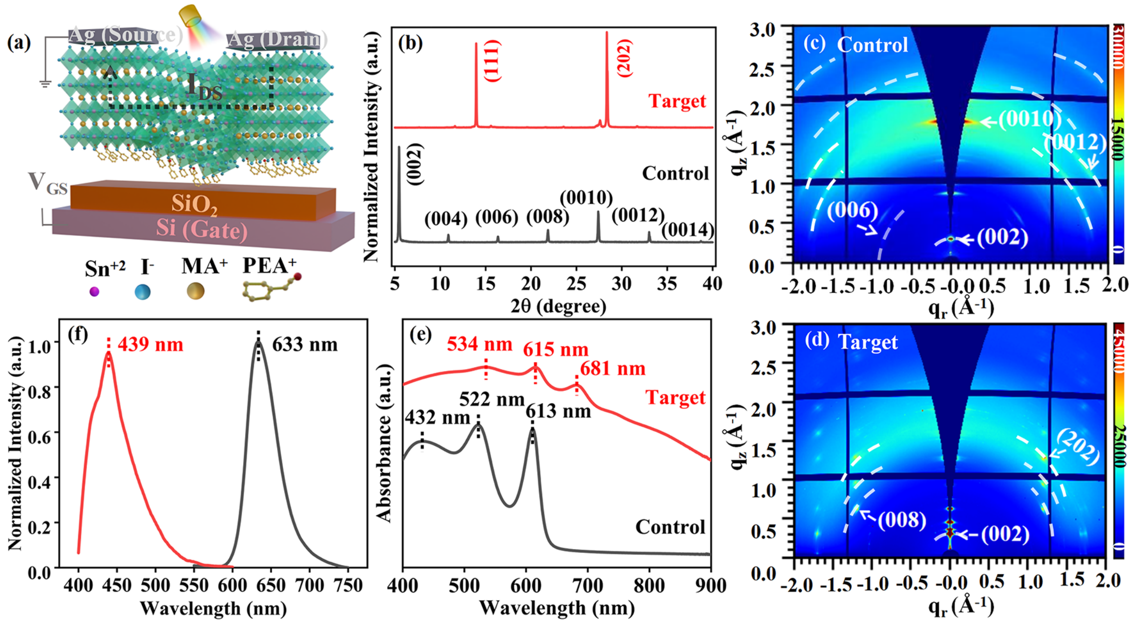

Figure 1. Characterizations of $(PEA)_2SnI_4$ and $(PEA)_2MA_6Sn_7I_{22}$ films. (a) Device structure of $(PEA)_2MA_6Sn_7I_{22}$ photoelectric transistor. (b) XRD patterns, (c, d) grazing incidence wide-angle X-ray scattering (GIWAXS) images, (e) UV−vis absorption spectra, and (f) PL spectra of $(PEA)_2SnI_4$ (control) and $(PEA)_2MA_6Sn_7I_{22}$ (target) films.

the electronic transport and device performance of 2D Sn-based perovskites can be enhanced.[20,21]

In this study, the effects of the dimensionality (n value) on the performance of 2D $(PEA)_2MA_{n-1}Sn_nI_{3n+1}$ perovskites and their photoelectric transistors are investigated. The photoelectric performances of the photoelectric transistors are improved by adjusting the dimensionality and microstructure of the 2D $(PEA)_2MA_{n-1}Sn_nI_{3n+1}$ perovskites. The $(PEA)_2MA_6Sn_7I_{22}$-based photoelectric transistor exhibits an n-type charge transport and excellent electrical properties. Furthermore, a $(PEA)_2MA_6Sn_7I_{22}$-based photoelectric transistor is integrated into a photoelectric controlled metal−oxide−semiconductor (MOS) inverter for logic transfer.

2. EXPERIMENTAL SECTION

2.1. Materials. Phenylethylammonium iodide (PEAI, 99.9%) is obtained from Advanced Election Technology Co., Ltd. Stannous iodide (SnI_2, 99.0%) is obtained from Macklin. Methylammonium iodide (MAI, 99.0%) is obtained from Xi'an Baolaite Co., Ltd. *N*,*N*-Dimethylformamide (DMF, 99.9%) and dimethyl sulfoxide (DMSO, 99.9%) are purchased from Merck. Anhydrous ethanol (ETOH, 99.7%), isopropyl alcohol (IPA, 99.7%), and acetone (AC, 99.5%) are purchased from Sinopharm Chemical Reagent Co., Ltd. All chemicals and solvents are used as received without further purification.

2.2. Device Fabrication. The p-type heavily doped Si substrate with SiO_2 dielectric layer (200 nm, 30 $nF\cdot cm^{-2}$) is ultrasonically cleaned using detergent, deionized water, anhydrous ethanol, acetone, and isopropyl alcohol for 15 min in that order. Subsequently, the Si/SiO_2 substrate is dried with nitrogen and treated with ultraviolet ozone for 30 min. A precursor perovskite solution is prepared by mixing PEAI, MAI, and SnI_2 at a molar ratio of $2:(n-1):(3n+1)$ (n = 1−8) in DMF/DMSO (4:1, v/v) under stirring for 4 h at 70 °C. The as-prepared precursor solution is filtered using a 0.22 μm polytetrafluoroethylene filter before use. The filtered precursor solution is spin-coated onto the Si/SiO_2 substrate for 40 s at 4000 rpm and then annealed at 100 °C for 10 min. Finally, a 200 nm Ag source/drain electrode is thermally evaporated using a metal shadow mask. The channel length and width are 50 and 500 μm, respectively. All operations are performed in an N_2 glovebox at room temperature.

2.3. Characterizations. The crystal structure of the 2D perovskite is characterized by X-ray diffraction (XRD, SmartLab, Rigaku) with Cu Kα radiation. The surface morphologies of the perovskite films are analyzed by scanning electron microscopy (SEM, S-4800, Hitachi, Japan). Ultraviolet−visible (UV−vis) absorption spectra are recorded on an Agilent Cary 5000 UV−vis spectrophotometer in the 400−900 nm range. The steady-state photoluminescence (PL) spectra are obtained using Spectrofluorometer FS5 (Edinburgh Instruments Ltd.) with the excitation wavelength λ_{ex} of 370 and 435 nm for $(PEA)_2SnI_4$ and $(PEA)_2MA_6Sn_7I_{22}$, respectively. The surface potential is measured via Kelvin probe force microscopy (KPFM, NT-MDT, Russia). All electrical characteristics are measured in a N_2 glovebox at room temperature using a semiconductor parameter analyzer (TH1991, Tonghui, Jiangsu) at the probe station.

3. RESULTS AND DISCUSSION

3.1. Characterizations of 2D $(PEA)_2MA_{n-1}Sn_nI_{3n+1}$ Perovskite. Photoelectric transistors are representative semiconductor devices that convert optical signals into electrical signals.[22] A 2D tin halide perovskite-based photoelectric transistor is constructed in a simple architecture with a bottom gate top contact (BGTC) configuration,[23] as shown in Figure 1a. $(PEA)_2MA_{n-1}Sn_nI_{3n+1}$ (n = 1, 2, 3, 4, 5, 6, 7, and 8) is spin-coated onto the dielectric layer (200 nm SiO_2) as an active layer using a one-step spin-coating method. A p-type heavily doped silicon (Si) wafer (525 μm) is used as the substrate. Ag is deposited on the $(PEA)_2MA_{n-1}Sn_nI_{3n+1}$ active layer via vacuum evaporation as the drain and source electrodes with a thickness of 200 nm. From the optical microscope image of the actual measured device (Figure S1), the width (W) and length

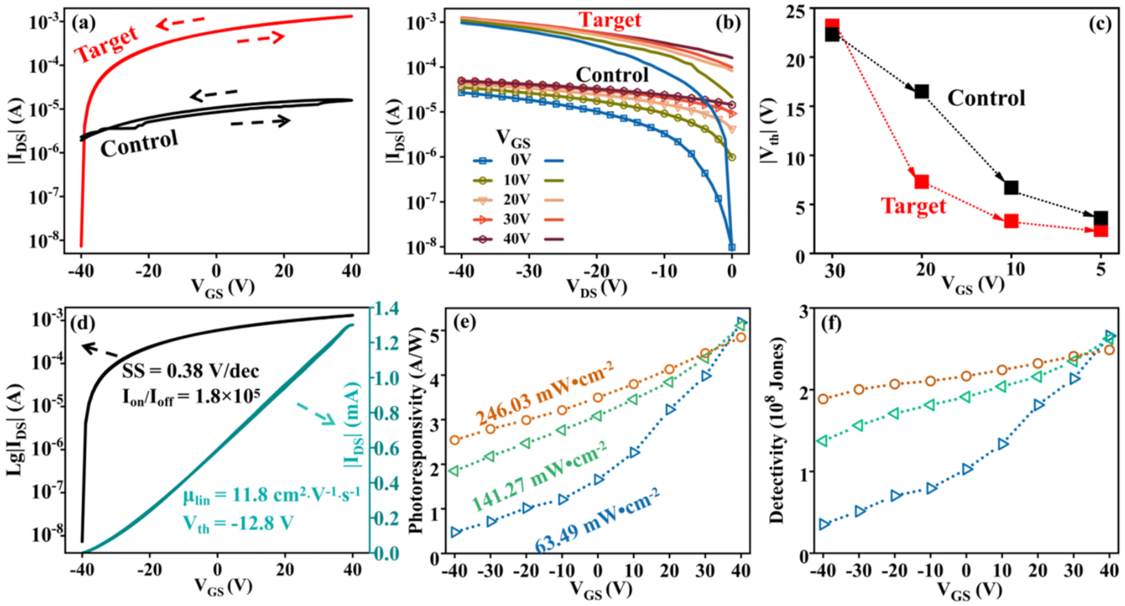

Figure 2. Photoelectric characteristics of control ($(PEA)_2SnI_4$) and target ($(PEA)_2MA_6Sn_7I_{22}$) devices. (a) Transfer characteristics of control ($(PEA)_2SnI_4$) and target ($(PEA)_2MA_6Sn_7I_{22}$) photoelectric transistors under illumination with a power intensity of 158.7 $mW \cdot cm^{-2}$ at $V_{DS} = -40$ V. (b) Output characteristic curves of control and target photoelectric transistors with different V_{GS} values under illumination. (c) Extracted threshold voltages under various gate electrochemical potentials (V_{GS}). When V_{GS} is 30, 20, 10, and 5 V, the corresponding V_{DS} is −30, −20, −10, and −5 V, respectively. (d) Semilog and linear plots of transfer characteristics for extracting target photoelectric transistor parameters, $V_{DS} = -40$ V. Variations in (e) photoresponsivity (R) and (f) detectivity (D^*) of target photoelectric transistor with bias voltage under illumination at different power intensities.

(L) of the channel are 500 and 50 μm, respectively. Figure S2 shows the transfer characteristic curve of different $(PEA)_2MA_{n-1}Sn_nI_{3n+1}$ devices, in which the drain-source current (I_{DS}) of the $(PEA)_2MA_6Sn_7I_{22}$ (n = 7)-based photoelectric transistor reaches a maximum of 1.28×10^{-3} A, thus indicating a higher photocurrent response compared with the other devices. Hereinafter, $(PEA)_2MA_6Sn_7I_{22}$ with n = 7 and $(PEA)_2SnI_4$ with n = 1 are referred to as the target and control samples, respectively.

Scanning electron microscopy (SEM) images in Figure S3 show that the $(PEA)_2MA_6Sn_7I_{22}$ film exhibits square blocks with larger crystal grains than the $(PEA)_2SnI_4$ film, which is consistent with the atomic force microscopy (AFM) image shown in Figure S3c. The larger crystal grain size of the $(PEA)_2MA_6Sn_7I_{22}$ film contributes to its excellent electrical performance in the phototransistor. A layered target film structure is desirable for the horizontal charge transport in transistors. The cross-sectional image shows a distinct and well-defined borderline between SiO_2 and perovskite layers, and the thickness of $(PEA)_2SnI_4$ and $(PEA)_2MA_6Sn_7I_{22}$ film is 0.33 and 1.07 μm, respectively (Figure S4). The layer structure of $(PEA)_2MA_6Sn_7I_{22}$ will make the film thicker. In combination with the previous electrical performance test, the appropriate film thickness will enhance the absorption of light and facilitate more efficient charge transport, thereby improving the photoelectric performance.

The structural dimensionality (i.e., n value) of 2D perovskites affects the electrical performance of the transistor; X-ray diffraction (XRD) is used to investigate the structural properties of the $(PEA)_2MA_6Sn_7I_{22}$ (target) and $(PEA)_2SnI_4$ (control) films, and the results are shown in Figure 1b. For $(PEA)_2SnI_4$, the diffraction peaks at 5.47, 10.89, 16.34, 21.87, 27.40, 33.01, and 38.79° correspond to the (002), (004), (006), (008), (0010), (0012), and (0014) lattice planes, respectively, thus indicating that (00l) reflections are dominant and $(PEA)_2SnI_4$ film grows parallel to the substrate.[14,24,25] For $(PEA)_2MA_6Sn_7I_{22}$, two strong diffraction peaks are observed at 13.96 and 28.35°, which correspond to the (111) and (202) lattice planes,[26,27] respectively. This suggests that the perovskite grows in a direction perpendicular to the substrate at larger n values. The crystal orientation of $(PEA)_2SnI_4$ and $(PEA)_2MA_6Sn_7I_{22}$ is further confirmed via grazing incidence wide-angle X-ray scattering (GIWAXS). As shown in Figure 1c,d, the sharp and discrete Bragg spots in $(PEA)_2SnI_4$ and $(PEA)_2MA_6Sn_7I_{22}$ films indicate excellent crystallinity and well-aligned perovskite structure. In the $(PEA)_2SnI_4$ film, high-intensity (00l) diffraction peaks along the q_z direction are observed, suggesting a preferred parallel orientation of these planes, which is consistent with the XRD results discussed above. The parallel-oriented crystals of $(PEA)_2SnI_4$ could hinder the charge transport and decrease the device performance.[28−30] The diffraction peaks of (111) and (202) in $(PEA)_2MA_6Sn_7I_{22}$ show that the oriented 2D perovskite crystals grew vertically to the substrate, forming a favorable charge transport channel to enhance the device performances.[31,32] The optical properties of the $(PEA)_2SnI_4$ and $(PEA)_2MA_6Sn_7I_{22}$ films were investigated via ultraviolet−visible (UV−vis) absorption and normalized photoluminescence (PL). As shown in Figure 1e, the control sample exhibits three absorption peaks at 432, 522, and 613 nm, which represent the formation of a 2D layered $(PEA)_2SnI_4$ film originating from strong quantum and dielectric confinement effects.[33,34] By introducing MA cations, the $(PEA)_2MA_6Sn_7I_{22}$ film exhibits stronger absorption from 400 to 900 nm, and the absorption peaks red-shift to 534, 615, and 681 nm. The bandgap energy (E_g) of the $(PEA)_2MA_{n-1}Sn_nI_{3n+1}$ thin films is calculated using Tauc's plot (Figure S5). For $(PEA)_2SnI_4$ and $(PEA)_2MA_6Sn_7I_{22}$, E_g decreases from 1.94 to 1.54 eV, thus indicating that $(PEA)_2MA_6Sn_7I_{22}$ exhibits a weaker quantum confinement effect when the number of inorganic metal halide layers increases with n.[7] As shown in Figure 1f, the PL spectra show a single peak for $(PEA)_2SnI_4$ and $(PEA)_2MA_6Sn_7I_{22}$, with emission peaks at 633 and 439 nm, respectively. Meanwhile, the peak area of $(PEA)_2MA_6Sn_7I_{22}$ is 61.03 larger than that (50.17) of $(PEA)_2SnI_4$, as shown in Table S1, thus indicating that the carriers in $(PEA)_2MA_6Sn_7I_{22}$ have released energy primarily through radiative recombination.[35]

3.2. Photoelectric Modulating 2D Perovskite Photoelectric Transistor.

The photoelectric performance of the $(PEA)_2MA_{n-1}Sn_nI_{3n+1}$ photoelectric transistors is further evaluated. Figures 2a and S6a show the transfer characteristic curves of the control and target photoelectric transistors under light and dark conditions. The source-drain currents (I_{DS}) of both the control and target devices increase with positive V_{GS} under negative V_{DS}, thus presenting the typical n-channel transport mode[36] (Figure S6a). Hysteresis effects are clearly observed in both devices under dark condition when V_{GS} is swept from −40 to 40 V and back to −40 V. After illuminating with a power intensity of 158.7 $mW{\cdot}cm^{-2}$ at $V_{DS} = -40$ V (Figure 2a), the dual-sweep transfer curve of the target photoelectric transistor coincides exactly without hysteresis and the I_{DS} at $V_{GS} = 40$ V reaches 1.3×10^{-3} A, which is ∼100 times higher than that of the control device (1.5×10^{-5} A). This can be attributed to the photoconductive effects. Similarly, as shown in Figures 2b and S6b,c, the output characteristics of the control and target devices exhibit n-type transistor characteristics under dark and light conditions, with both linear and saturation regions presented. When the same V_{GS} is applied, the I_{DS} of the two devices increases distinctly as V_{DS} is swept from 0 to −40 V under dark and illumination, while the transistor characteristics are retained. Meanwhile, the $|I_{DS}|$ of the target device at $V_{GS} = 40$ V and $V_{DS} = -40$ V reaches 1.2×10^{-3} A, which is ∼30 times higher than that of the control device (4.9×10^{-5} A) in the illuminated condition. These results indicate that the higher I_{DS} of the target photoelectric transistor is attributed to the photoelectric conversion process under illumination,[37,38] which implies that the target device exhibits excellent photoelectric response behaviors. To evaluate the stability and reproducibility, performance tests on 6 batches of devices are conducted. As shown in Figure S7 and Table S2, the standard deviation of performance parameters across different batches is less than 0.1, exhibiting a high level of consistency in device performance from batch to batch and validating the robustness of our fabrication process.

The threshold voltage (V_{th}) is the voltage at which the transistor is activated and is an important metric for evaluating the performance of transistors and logic circuits.[39] V_{th} is obtained from the axis intercept of V_{GS} in the linear extrapolation of the transfer characteristic curve at its maximum first derivative (slope) point (the point of maximum transconductance, g_m).[40] As presented in Figure 2c, the V_{th} of the control and target photoelectric transistors increases with positive V_{GS}, which is consistent with the findings reported in the literature.[41] The shifts in V_{th} are attributed to the charge trapping in the semiconductor (interface) under illuminated conditions.[42] When 20 V of V_{GS} is applied, the V_{th} absolute value of the control and target device is 16.5 and 7.3 V, respectively, thus indicating that the V_{th} of $(PEA)_2MA_{n-1}Sn_nI_{3n+1}$ photoelectric transistors can be modulated by different n values. Meanwhile, a lower V_{th} of the target device is beneficial for improving the switching speed between the on and off states, thus reducing the energy consumption and enhancing the operating frequency and response ability.[22,43]

Considering the higher I_{DS} in the transfer and output characteristic curves and the lower V_{th} absolute value, the target ($(PEA)_2MA_6Sn_7I_{22}$) photoelectric transistor is primarily investigated in this study. The I_{on}/I_{off} ratio, linear mobility (μ_{lin}), and subthreshold swing (SS) are important parameters for evaluating the performance of photoelectric transistors. Because $|V_{GS}-V_{th}| > V_{DS}$, μ_{lin} can be expressed from the I_{DS}−V_{GS} curve according to the equation[36,44,45]

$$I_{Dlin} = C_i \mu_{lin} \frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2\right] \tag{1}$$

where C_i is the capacitance per unit area of the dielectric, and W and L are the channel width and length, respectively. The SS is obtained from the subthreshold region of the $\log(I_{DS})-V_{GS}$ curve using the following equation[46,47]

$$SS = \frac{dV_{GS}}{d(\lg I_{DS})} \tag{2}$$

A smaller SS indicates that a slight change in V_{GS} can change the current significantly, suggesting a faster on-/off-switching speed.[48] As shown in Figure 2d, the I_{on}/I_{off} ratio, V_{th}, μ_{lin}, and SS of the target device under light illumination are 1.8×10^5, −12.8 V, 11.8 $cm^2{\cdot}V^{-1}{\cdot}s^{-1}$, and 0.38 $V{\cdot}dec^{-1}$, respectively. Compared with the reported 2D halide perovskite transistors in Figure S8, the $(PEA)_2MA_6Sn_7I_{22}$ transistor has the lowest SS and exhibits better gate-controlled ability and a higher on-/off-switching speed.

To further evaluate the photoelectric response of the target transistor, the photoresponsivity (R), detectivity (D^*), and photosensitivity (S) as a function of V_{GS} ranging from −40 to 40 V under different light power intensities are characterized. The photoresponsivity reflects the capability in terms of optical signals converted into electrical current and can be expressed as[49,50]

$$R = \frac{I_{photo}}{P_{ill} \times A} \tag{3}$$

where I_{photo} is the photocurrent, P_{ill} is the incident light intensity, and S represents the effective area of the conductive channel in the photoelectric transistor. D^* reflects the strength of the device's detection ability and is determined by the photoresponsivity and dark current density as follows[51,52]

$$D^* = \frac{R}{\sqrt{2qJ_{dark}}} \tag{4}$$

where q is the elementary charge and J_{dark} is the dark current density. As depicted in Figure 2e,f, R and D^* are closely related to V_{GS} and increase monotonically as V_{GS} increases from −40 to 40 V under different light intensities, which is attributed to the gain caused by the photogating effect.[53,54] Both R and D^* reach the maximum values of 5 $A{\cdot}W^{-1}$ and 2.6×10^8 Jones, respectively, at a low incident power density of 63.49 $mW{\cdot}cm^{-2}$ at $V_{GS} = 40$ V, thus indicating that the target photoelectric transistor exhibits good photoelectric response under low light intensity. Moreover, the photosensitivity increases significantly with the light power intensity[55] (Figure S9). The photoelectrical performances of the phototransistors

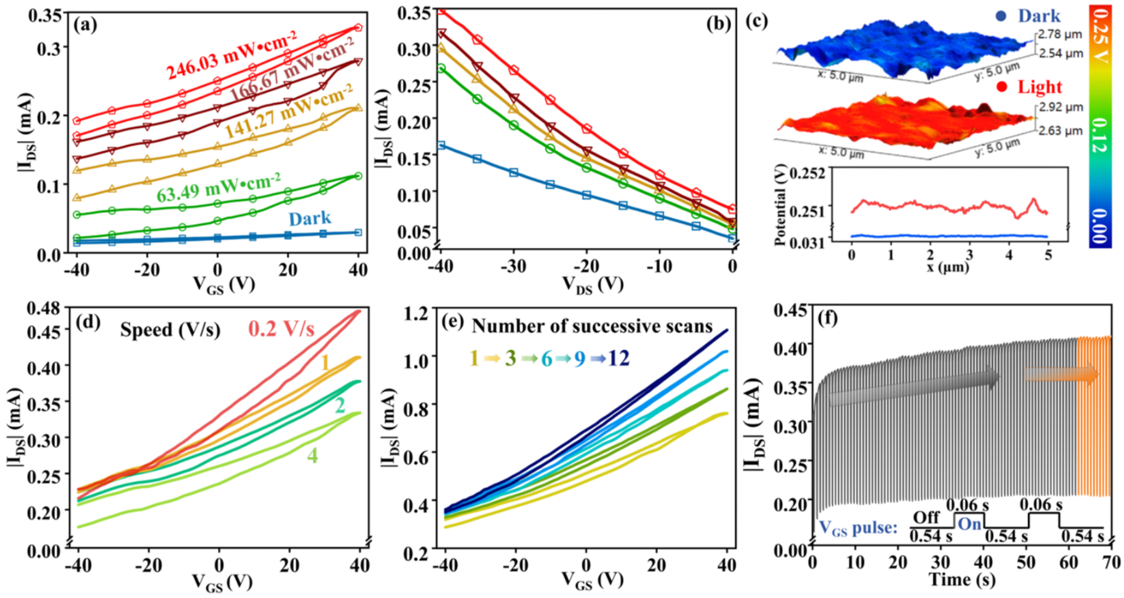

Figure 3. Photoelectronic performances of the $(PEA)_2MA_6Sn_7I_{22}$ (target) photoelectric transistor. (a, b) Transfer and output characteristic curves of the target photoelectric transistor under different light intensities. (c) Three-dimensional (3D) topography images of $(PEA)_2MA_6Sn_7I_{22}$ film (5 μm × 5 μm) under dark and light conditions overlaid by surface potential. (d, e) Transfer characteristics of target transistor with various V_{GS} scanning speeds and number of successive scans. (f) Cycle-dependent switching characteristic curve of target transistor under 0.06 s of V_{GS} pulse.

are summarized in Figure S10 and Table S3. When the number of layers is 7, the $(PEA)_2MA_6Sn_7I_{22}$-based photoelectric transistor exhibits the best device performance, elaborating that the photoelectrical performances of the phototransistors can be controlled by adjusting the number of 2D perovskite layers.[56,57]

The photoelectric behavior of the target photoelectric transistor is further systematically investigated by exploring the photocurrent at various light power intensities, scanning rates, and cycles. Figure 3a shows the photocurrents at different V_{GS} and light power values at 405 nm. The target device can generate a maximum photocurrent of 0.11 mA under an optical power of 63.49 mW·cm^{-2} and a bias of 40 V. As the light power intensity increases from 63.49 to 246.03 mW·cm^{-2}, the photocurrent increases gradually from 0.11 to 0.33 mA. Similarly, the photocurrent shown in the output characteristic curve increases gradually with the light intensity (Figure 3b). This signifies that the target photoelectric transistor exhibits different degrees of photoelectric response under different light intensities, because the density of photogenerated charge carriers is proportional to the light power intensities.[58,59] To demonstrate this photoelectric response, the surface potential of the $(PEA)_2MA_6Sn_7I_{22}$ film is determined by using Kelvin-probe force microscopy (KPFM). As presented in Figures 3c and S11, the surface mean potentials of the $(PEA)_2MA_6Sn_7I_{22}$ film before and after light irradiation are 0.03 and 0.25 V, respectively. A relatively higher surface potential appears under light illumination because the perovskite can absorb photons and generate photogenerated charge carriers,[60,61] whereas photogenerated holes and electrons accumulate on the perovskite film surface and perovskite/SiO_2 interface, respectively. To gain a deep understanding of the charge transfer processes, a plausible operation mechanism in our photoelectric transistor is illustrated in Figure S12. $(PEA)_2MA_6Sn_7I_{22}$ perovskite and SiO_2 are arranged in a type-IV band alignment. A large number of photogenerated electrons and holes are generated in $(PEA)_2MA_6Sn_7I_{22}$ under light illumination. Type IV heterointerface effectively prevents the electron transfer from perovskite to SiO_2 and allows holes to transport through the interface by tunneling. The photogenerated electrons will transfer to Ag electrode. Therefore, light illumination can enhance the electron-trapping capacity and photocurrent, thus resulting in an excellent photoelectric response of the target device.

Figure 3d shows the transfer characteristic curves acquired at different V_{GS} scanning speeds. When the scanning speed of V_{GS} increases from 0.2 to 4 V·s^{-1} as scanning is performed from −40 to 40 V, the I_{DS} decreases gradually from 0.47 to 0.33 mA. This suggests that the speed of ion migration is diminished and the mobile ionic species may have fewer opportunities to remigrate to their equilibrium state, thus resulting in a lower I_{DS}.[62,63] Moreover, the I_{DS} increases gradually with the number of scanning tests (Figure 3e), which is consistent with the literature.[64] This is primarily due to the holes trapped in $(PEA)_2MA_6Sn_7I_{22}$, which prolongs the recombination time of the photogenerated carriers. To further substantiate the potential of this $(PEA)_2MA_6Sn_7I_{22}$-based transistor, its on- and off-switching behaviors are investigated. Figure 3f presents the reproducible I_{DS} response to switching of the V_{GS} pulse under light illumination. As shown, I_{DS} increases rapidly when 40 V of V_{GS} is applied (0.06 s), after which it returns to its initial state when V_{GS} is removed. When this cycle is repeated for 62 s, the maximum value of I_{DS} increases gradually owing to ion migration.[62,65] Subsequently, I_{DS} remains constant, thus indicating that the target photoelectric transistor exhibits reliable and reproducible I_{DS} switching behavior. Moreover, the stability of the target photoelectric transistor has a crucial influence on the device performance, which can further determine the practical application. When the target photoelectric transistor is stored in an N_2 glovebox for 15 days (Figure S13), the electron mobility of the device remains almost constant at 5.96 cm^2·V^{-1}·s^{-1}, suggesting the good resistance to aging under the tested conditions.

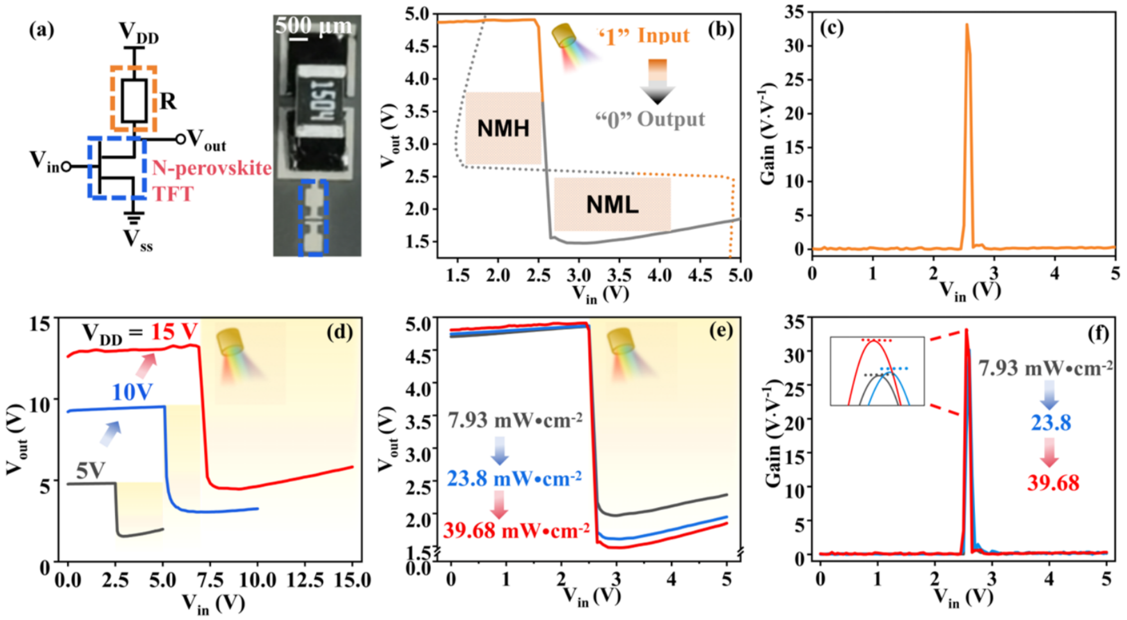

Figure 4. Performance of photoelectric controlled MOS inverter. (a) Equivalent electronic circuit and photographs of the inverter. (b, c) Voltage transfer characteristic and gain curves of the inverter. The two shaded boxes show noise margin extraction using the maximum equal criterion (MEC) method from the butterfly plot. (d) Voltage transfer characteristics of the photoelectric controlled inverter as a function of supply voltage (V_{DD}). Voltage transfer characteristic (e) and gain (f) curves under different light intensities at V_{DD} = 5 V. The inset is a partial enlargement of the gain from 20 to maximum.

3.3. Performance of Photoelectric Controlled MOS Inverter.

Among the diverse circuit components, inverters are widely considered as the fundamental element. Additionally, the applicability of 2D perovskite devices to logic electronics must be evaluated. Therefore, a simple unipolar resistive-load inverter (photoelectric controlled MOS inverter) is constructed by connecting the $(PEA)_2MA_6Sn_7I_{22}$ photoelectric transistor with a 1.36 MΩ resistor. A digital circuit diagram and a photograph of the inverter are shown in Figure 4a, where V_{DD}, V_{in}, V_{out}, and V_{ss} represent the supply voltage, input voltage, output voltage, and voltage source supply, respectively. V_{out} remains primarily unchanged when V_{in} ranges from 0 to 5 V in the dark, indicating that the inverter does not amplify the signal (Figure S14). Therefore, the voltage transfer curve is tested in the dark when V_{in} is less than 2.5 V ($V_{DD}/2$, V_{DD} = 5 V) and under light illumination when V_{in} ranges from 2.5 to 5 V. A high V_{in} is equivalent to logic "1", whereas a low V_{out} is equivalent to logic "0", and vice versa. As shown in Figure 4b, V_{out} decreases abruptly from 4.9 to 1.5 V at V_{in} = 2.5 V when the light is turned on, indicating an ideal logic transfer from "1" to "0". The inverter exhibits a standard rail-to-rail voltage transfer characteristic.[66] These results indicate that the logic transfer of this inverter can be realized via light modulation. When V_{in} is 3−5 V, V_{out} increases slightly; this is due to the fact that the phototransistor reaches the saturation state and the current does not continue to increase. The ability of the charge trap to capture the hole increases after the continuous application of light, the trap recombination increases, resulting in the current decreasing. Finally, V_{out} increases and the curve shows an upward trend.[67,68] The butterfly voltage transfer curve plot with a square, as shown in Figure 4b, is used to calculate the noise margin based on the maximum equal criterion (MEC) method,[7] whereas another dotted voltage transfer curve is plotted in a mirror. The high noise margin (NMH) is calculated to be 2.2 V at V_{DD} = 5 V, which is 88% of the ideal value ($V_{DD}/2$). The low noise margin (NML) is calculated to be 0.88 V at V_{DD} = 5 V. This demonstrates that even if the noise causes a V_{in} shift of 2.2 V in every direction, the inverter can still output the correct V_{out} signal. Additionally, the inverter exhibits a high gain of 33 at V_{DD} = 2.5 V (Figure 4c) owing to the high mobility, small subthreshold swing, and reliable stability of the photoelectric transistors.[69] The on-power consumption (P) is determined by the supply voltage (V_{DD}) and conduction current (I_{DD}) and calculated to be 18 μW. The electrical performance parameters of the photoelectric controlled MOS inverter are shown in Table S4. This high-gain photoelectrically controlled MOS inverter with low energy consumption is applicable to portable electronic circuits.

The signal inverting behaviors of this photoelectric controlled inverter are further demonstrated under different V_{DD}, light intensity, and load resistance values. As shown in Figure 4d, the device guarantees either a high or a low output voltage at different input voltages and achieves the logic transfer from "0" to "1". The output current decreases with V_{DD} (Figure S15a), and the on-power consumption decreases from 174 to 18 μW. Meanwhile, a higher gain is obtained at a lower V_{DD} (Figure S15b). Figure 4e depicts the effect of the light intensity on the voltage transfer characteristics. When the light intensity increases from 7.93 to 39.68 mW·cm^{-2}, V_{out} decreases from 2.2 to 1.5, and the gain increases from 26.5 to 30.2 (Figure 4f), which is attributed to the increased density of the photogenerated charge carrier with increasing light intensity. This implies that a higher light intensity is beneficial for improving the electrical performance of the device. Additionally, the circuit performance can be adjusted by the load resistance (Figure S16). The output current decreases, resulting in the decrease of the power density with the increase of load resistance, indicating that the power density can be flexibly controlled by the load resistance (Figure S17). These results present that the photoelectric controlled MOS inverter exhibit good stability.

4. CONCLUSIONS

In conclusion, 2D perovskite $(PEA)_2MA_{n-1}Sn_nI_{3n+1}$ is successfully prepared by introducing large PEA cations. $(PEA)_2MA_6Sn_7I_{22}$ shows a weaker quantum confinement effect as the number of inorganic metal halide layers increases with n. The $(PEA)_2MA_6Sn_7I_{22}$ (n = 7) photoelectric transistor shows n-type charge transport and excellent electrical properties, with a mobility of 11.8 $cm^2 \cdot V^{-1} \cdot s^{-1}$, low subthreshold swing (SS) of 0.38 $V \cdot decade^{-1}$, photoresponsivity (R) of 5 $A \cdot W^{-1}$, and detectivity (D^*) of 2.6×10^8 Jones. The standard deviation of performance parameters across 6 batches is less than 0.1, exhibiting a high level of consistency in device performance from batch to batch and good reproducibility. When stored in an N_2 glovebox for 15 days, the electron mobility of the device remained almost constant at 5.96 $cm^2 \cdot V^{-1} \cdot s^{-1}$, confirming their good long-term reliability. The gain of the inverter was still maintained at 30, exhibiting remarkable stability under varying test conditions. Based on the photoelectric performances of the $(PEA)_2MA_6Sn_7I_{22}$ photoelectric transistor, a photoelectric controlled MOS inverter is constructed to convert the logic value. Unlike previous inverters prepared via complex processes based on patterned masks, this photoelectronic controlled MOS inverter is constructed by connecting the $(PEA)_2MA_6Sn_7I_{22}$ photoelectric transistor with a resistor, which consumes a low on-power consumption of 18 μW. The $(PEA)_2MA_6Sn_7I_{22}$ phototransistors of high-performance and low-power show great potential in the field of miniaturized integrated circuits and logic circuits and have excellent practical prospects.

■ ASSOCIATED CONTENT

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.5c10965.

> Transfer characteristic curves of $(PEA)_2MA_{n-1}Sn_nI_{3n+1}$ (n = 1, 2, 3, 4, 5, 6, 7, and 8) phototransistors; SEM and AFM planar and cross-sectional morphologies of $(PEA)_2SnI_4$ and $(PEA)_2MA_6Sn_7I_{22}$; band gap of $(PEA)_2SnI_4$ and $(PEA)_2MA_6Sn_7I_{22}$; transfer characteristic curves of $(PEA)_2SnI_4$ phototransistor and $(PEA)_2MA_6Sn_7I_{22}$ phototransistor under light and dark; comparison of the subthreshold swing (SS) of different 2D halide perovskite transistors; photosensitivity of $(PEA)_2MA_6Sn_7I_{22}$ phototransistor; voltage transfer characteristic of the inverter in dark; current transfer characteristic curve and gain under different V_{DD}; voltage and current transfer characteristic curves and gains under different load resistance values R; and obtained unimodal integral area from perovskite photoluminescence (PL) (PDF)

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Notes

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